CLAIMS

What is claimed is:

1. A semiconductor device assembly, comprising:

at least one semiconductor device; and

a plurality of mutually laterally spaced discrete spacers protruding from a surface of said at least one semiconductor device, said spacers defining a distance said surface of said at least one semiconductor device is to be spaced apart from another semiconductor device to be positioned in superimposed relation with said at least one semiconductor device.

2. The semiconductor device assembly of claim 1, wherein at least one of said spacers is resiliently compressible.

3. The semiconductor device assembly of claim 1, wherein at least one of said spacers protrudes from an active surface of said at least one semiconductor device.

4. The semiconductor device assembly of claim 3, wherein each of said spacers protrudes from an active surface of said at least one semiconductor device.

5. The semiconductor device assembly of claim 4, wherein said plurality of spacers are arranged to stably support said another semiconductor device.

6. The semiconductor device assembly of claim 1, further comprising:

said another semiconductor device positioned adjacent said spacers, opposite from said at least one semiconductor device.

7. The semiconductor device assembly of claim 6, further comprising:

adhesive material between said at least one semiconductor device and said another semiconductor device.

8. The semiconductor device assembly of claim 7, wherein said adhesive material is located between adjacent spacers.

9. The semiconductor device assembly of claim 6, wherein said spacers are electrically isolated from internal circuitry of said at least one semiconductor device.

10. The semiconductor device assembly of claim 1, wherein said spacers comprise electrically conductive material.

11. The semiconductor device assembly of claim 10, wherein said spacers communicate with a ground plane of said at least one semiconductor device.

12. The semiconductor device assembly of claim 1, further comprising:
a substrate with which at least one semiconductor device is associated.

13. The semiconductor device assembly of claim 12, wherein said substrate comprises at least one of a circuit board, an interposer, a semiconductor device, and leads.

14. The semiconductor device assembly of claim 12, wherein at least one bond pad of said at least one semiconductor device is in communication with a corresponding contact area of said substrate.

15. The semiconductor device assembly of claim 14, further comprising:
at least one discrete conductive element extending from said at least one bond pad, over an active surface of said at least one semiconductor device, to said corresponding contact area.

16. The semiconductor device assembly of claim 15, wherein heights of said spacers exceed a maximum height said at lea st one discrete conductive element protrudes above said active surface.

17. The semiconductor device assembly of claim 1, wherein said spacers are secured to noncircuit bond pads of said at least one semiconductor device.

18. A semiconductor device assembly, comprising:

a substrate;

a first semiconductor device associated with said substrate, bond pads of said first semiconductor device in communication with corresponding contact areas of said substrate;

mutually laterally spaced discrete spacers positioned on and protruding from an active surface of said first semiconductor device; and

a second semiconductor device comprising a back side positioned on said mutually laterally spaced discrete spacers.

19. The semiconductor device assembly of claim 18, wherein said substrate comprises one of a circuit board, an interposer, another semiconductor device, and leads.

20. The semiconductor device assembly of claim 18, wherein said bond pads and said corresponding contact areas comminicate by way of discrete conductive elements positioned therebetween.

21. The semiconductor device assembly of claim 20, wherein said discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads.

22. The semiconductor device of claim 18, wherein said mutually laterally spaced discrete spacers are secured to noncircuit bond pads of said first semiconductor device.

23. The semiconductor device assembly of claim 22, wherein said laterally discrete spacers comprise conductive material.

24. The semiconductor device assembly of claim 23, wherein said mutually laterally spaced discrete spacers are electrically isolated from internal circuitry of said first semiconductor device.

25. The semiconductor device assembly of claim 23, wherein said mutually laterally spaced discrete spacers are in communication with a ground or reference voltage plane of said first semiconductor device.

26. The semiconductor device assembly of claim 25, wherein said back side of said second semiconductor device is also in communication with said ground or reference voltage plane.

27. The semiconductor device assembly of claim 20, wherein heights of said laterally discrete spacers exceed a maximum height said discrete conductive elements protrude above said active surface.

28. The semiconductor device assembly of claim 18, wherein at least one of said laterally discrete spacers is compressible.

29. The semiconductor device assembly of claim 18, wherein said second semiconductor device comprises a dielectric layer on at least portions thereof that contact said laterally discrete spacers.

30. The semiconductor device assembly of claim 18, wherein bond pads of said second semiconductor device communicate with corresponding contact areas of said substrate by way of discrete conductive elements positioned therebetween.

31. The semiconductor device assembly of claim 18, further comprising:
an adhesive layer between said first semiconductor device and said second semiconductor device.

32. The semiconductor device assembly of claim 31, wherein at least some of said mutually laterally spaced discrete spacers extend through said adhesive layer.

33. The semiconductor device assembly of claim 18, further comprising:
at least one additional semiconductor device positioned over said second semiconductor device.

34. The semiconductor device assembly of claim 18, further comprising:
an encapsulant material substantially covering said first semiconductor device, said second semiconductor device, said discrete conductive elements, and portions of said substrate located adjacent to said first semiconductor device.

35. The semiconductor device assembly of claim 18, further comprising:
at least one external connective element carried by said substrate and in electrical communication with at least one corresponding contact area of said substrate.

36. A method for assembling semiconductor devices in stacked arrangement, comprising:
providing a substrate;
securing a first semiconductor device to said substrate;
electrically connecting bond pads of said first semiconductor device to corresponding contact areas of said substrate;
positioning discrete spacers at mutually laterally spaced positions on at least one of an active surface of said first semiconductor device and a back side of said second semiconductor device;
positioning a second semiconductor device over said first semiconductor device, said spacers separating said first semiconductor device from said second semiconductor device.

37. The method of claim 36, wherein said providing comprises providing at least one of a circuit board, an interposer, another semiconductor device, and leads.

38. The method of claim 36, wherein said electrically connecting comprises placing discrete conductive elements between bond pads of said first semiconductor device and corresponding contact areas of said substrate.

39. The method of claim 38, wherein said placing comprises wire bonding.

40. The method of claim 38, wherein said placing comprises tape-automated bonding.

41. The method of claim 38, wherein said placing comprises thermocompression bonding leads between said bond pads and said corresponding contact areas.

42. The method of claim 36, wherein said positioning spacers comprises positioning resilient compressible spacers.

43. The method of claim 36, wherein said positioning spacers comprises securing spacers to noncircuit bond pads.

44. The method of claim 43, wherein said positioning spacers comprises positioning said spacers in electrical isolation from internal circuitry of said first semiconductor device.

45. The method of claim 43, wherein said positioning spacers comprises positioning spacers in communication with a ground plane of said first semiconductor device.

46. The method of claim 36, wherein said positioning said second semiconductor device comprises positioning said second semiconductor device with a back side thereof facing an active surface of said first semiconductor device.

47. The method of claim 36, further comprising:

electrically connecting bond pads of said second semiconductor device and corresponding contact areas of said substrate.

48. The method of claim 36, further comprising:

applying adhesive material at least to a surface of said first semiconductor device.

49. The method of claim 48, wherein said applying adhesive material comprises introducing adhesive material between said first and second semiconductor devices.

50. The method of claim 36, further comprising:

positioning at least one additional semiconductor device over said second semiconductor device.

51. The method of claim 36, further comprising:

substantially encapsulating said first semiconductor device, said spacers, said second semiconductor device, and portions of said substrate located laterally adjacent said first semiconductor device.

52. The method of claim 36, further comprising:

placing at least one external conductive element in communication with at least one corresponding contact area of said substrate.